

Silistix Joins OCP-IP

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PORTLAND, Ore— February 13, 2006 — Open Core Protocol International Partnership (OCP-IP) announces that Silistix has joined the Organization. Leveraging the advantages of OCP, the industry standard socket, Silistix intends to expand its product offering of revolutionary self-timed Chip-Area INterconnect (CHAIN) tools. Silistix is an EDA company developing software for the design and synthesis of self-timed interconnect logic for System-on-Chip designs that replace existing synchronous hierarchical bus structures, thereby reducing power consumption and accelerating timing closure and reuse. Silistix is a spin-out from the Amulet asynchronous-logic research group at the University of Manchester in Manchester, England. Silistix will develop OCP-compliant adaptors for initiators and targets of generated self-timed interconnects. This will allow existing endpoints such as processors, memory controllers, DMA controllers, and peripherals to interface with CHAIN fabrics without modification, thereby significantly reducing design time. “Network on Chip addresses many demanding challenges resulting from huge complexity of systems,” said Ian Mackintosh, President OCP-IP. “These challenges make reuse more critical than ever. OCP enables reuse regardless of chip architecture, interconnect approach or which processor cores are featured. These capabilities are further enhanced by technical advances such as Silistix’ CHAIN interconnect. We are delighted to have Silistix adopt and endorse OCP and we look forward to working with them in the future.” “The benefits of Silistix’ EDA approach to the looming interconnect crisis, while simultaneously solving several of the largest issues designers face today, makes it a natural fit for OCP users,” said David Fritz, VP of Marketing for Silistix. “We believe that by working with OCP-IP we can significantly extend the reach of our products into critical areas of the world market.” OCP-IP members receive free training, support, software tools, and documentation. This infrastructure allows IP and EDA vendors to eliminate the need to internally design, document, train and evolve a proprietary standard and set of support tools, which enables these vendors to focus their efforts and resources on the challenges of developing IP that can be quickly integrated and easily verified in a wide variety of SoC designs. As a result, IC design teams can better dedicate their critical resources to the design and delivery of products. About OCP-IP The Open Core Protocol International Partnership Association, Inc. (OCP-IP), formed in 2001, promotes and supports the Open Core Protocol (OCP) as the complete socket standard ensuring rapid creation and integration of interoperable virtual components. OCP-IP's Governing Steering Committee participants include: Nokia [NYSE: NOK], Texas Instruments [NYSE: TXN], Toshiba Semiconductor Group (including Toshiba America TAEC), and Sonics. OCP-IP is a non-profit corporation delivering the first fully supported, openly licensed, core-centric protocol comprehensively fulfilling system-level integration requirements. The OCP facilitates IP core reusability and reduces design time, risk, and manufacturing costs for SoC designs. VSIA endorses the OCP socket, and OCP-IP is affiliated with the VSI Alliance. For additional background and

membership information, visit www.OCPIP.org. About Silistix Silistix is a venture-funded spin-out of the University of Manchester, UK. The company's focus is on the development and deployment of EDA tools for the design and synthesis of self-timed interconnect technology for complex system-on-a-chip (SoC) communication. The company has offices in Manchester, England, San Jose, California, and Tokyo, Japan.

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